

# CLC014 Adaptive Cable Equalizer for High-Speed Data Recovery

## General Description

National's CLC014 adaptive cable equalizer is a low-cost monolithic solution for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The CLC014 simplifies the task of high-speed data recovery with a one-chip solution and a minimal number of external components. The equalizer automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 40 dB at 200 MHz. This corresponds to 300 meters of Belden 8281 or 120 meters of Category 5 UTP (unshielded twisted pair).

**The CLC014 provides superior jitter performance: 180ps<sub>pp</sub> for 270 Mbps data that has passed through 200 meters of Belden 8281 cable. This exceptional performance provides wide error margin in digital data links.** The equalizer operates on a single supply with a power consumption of only 290 mW. The small 14-pin SOIC package allows for high-density placement of components for multi-channel applications such as routers. The equalizer operates over a wide range of data rates from less than 50 Mbps to rates in excess of 650 Mbps.

The equalizer is flexible in allowing either single-ended or differential input drive. Its high common mode rejection provides excellent immunity to interference from noise sources. On-chip quantized feedback eliminates baseline wander.

Additional features include a carrier detect output and an output mute pin which, when tied together, mute the output when no signal is present. A buffered eye monitor output is provided, for viewing the equalized signal prior to the comparator. Differential AEC pins allow the user to set the inter-

nal adaptive loop time constant with one external capacitor. Also, the CLC014 is insensitive to the pathological patterns inherent in the video industry standards.

## Features

- Automatic equalization of coaxial and twisted pair cables
- Carrier detection and output mute
- Output eye monitor
- Single supply operation: +5V or -5.2V
- Single-ended or differential input
- Low cost

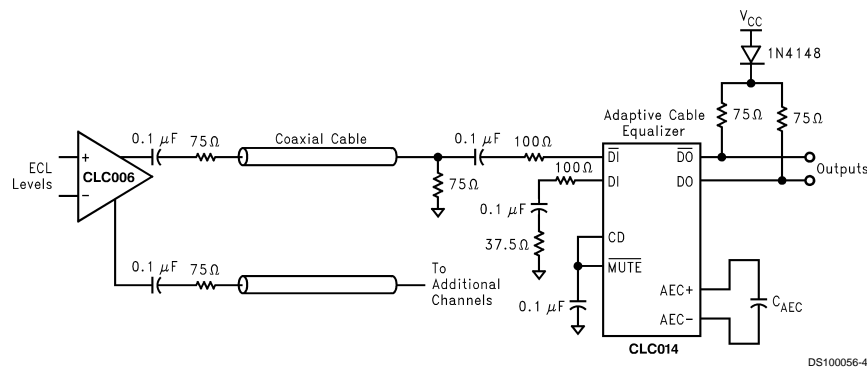
## Applications

- SMPTE 259M serial digital interfaces: NTSC/PAL, 4:2:2 component and wide screen; also 540 Mbps (4:4:4:4)
- Serial digital video routing and distribution
- Serial digital data equalization and reception
- Data recovery equalization: ATM, CAD networks, medical, set top terminals, industrial video networks

## Key Specifications

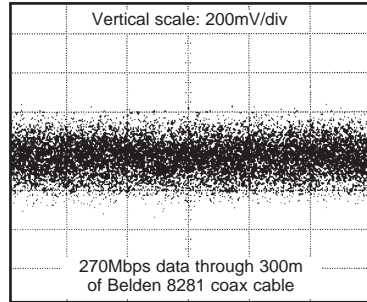
- Low jitter: 180ps<sub>pp</sub> @ 270 Mbps through 200 meters of Belden 8281 coaxial cable
- High data rates: < 50 Mbps to > 650 Mbps
- Excellent input return loss: 19 dB @ 270 MHz
- Low supply current: 58 mA
- Equalizes up to 300+ meters of Belden 8281 or 120 meters of Cat 5 UTP cable

## Typical Application



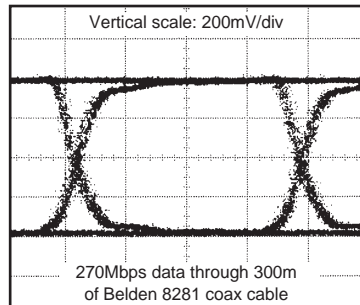
## Typical Application (Continued)

### Before Equalization



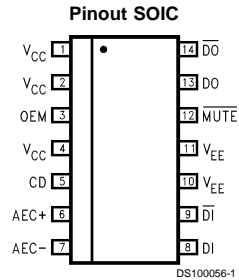
DS100056-2

### After Equalization



DS100056-3

## Connection Diagram



**14-Pin SOIC**  
**Order Number CLC014AJE**  
**See NS Package Number M14A**

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}-V_{EE}$ )	-0.3V, +6.5V
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 4 sec.)	+260°C
ESD Rating (Note 14)	<500V
$\theta_{JA}$ 14-Pin SOIC (AJE)	95°C/W
MTTF (based on limited life test data)	$4.8 \times 10^7$ hours

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}-V_{EE}$ )	4.5V to 5.5V
Operating Temperature Range	-40°C to +85°C
Series Input Resistance (In Series w/DI & $\overline{DI}$ )	100 $\Omega$
Input Coupling Capacitance	0.1 $\mu$ F
AEC Capacitor (Connected between AEC+ & AEC-)	50 pF to 1 $\mu$ F
Cable Input Voltage Swing (Note 4)	720 to 880 mV <sub>pp</sub>
DO/ $\overline{DO}$ Minimum Voltage (Note 15)	$V_{CC}-1.6V$

## Electrical Characteristics

( $V_{CC} = +5V$ ,  $V_{EE} = 0V$ , signal source swing =  $0.8 V_{pp}$ (Note 4),  $C_{AEC} = 100$  pF)

Parameter	Conditions	Typ +25°C	Min/Max +25°C	Min/Max -40°C to +85°C	Units
<b>DYNAMIC PERFORMANCE</b>					
<b>Residual Jitter</b>					
100 meters Belden 8281	270 Mbps PRN (Note 5)	150	250	400	ps <sub>pp</sub>
200 meters Belden 8281	270 Mbps PRN (Note 5)	180	250	400	ps <sub>pp</sub>
300 meters Belden 8281	270 Mbps PRN (Notes 3, 5)	350	500	750	ps <sub>pp</sub>
<b>Equalization Time Constant</b>					
100 meters Belden 8281	$C_{AEC} = 100$ pF (Note 6)	1.5	—	—	$\mu$ s
200 meters Belden 8281	$C_{AEC} = 100$ pF (Note 6)	2.0	—	—	$\mu$ s
300 meters Belden 8281	$C_{AEC} = 100$ pF (Note 6)	3.2	—	—	$\mu$ s
output rise and fall time (20%–80%)	$R_{collector} = 75\Omega$	750	—	—	ps
output duty cycle distortion		30	—	—	ps
minimum average transition density		1/50	—	—	trans/ns
maximum average data rate	150m Belden 8281 (Note 7)	650	—	—	Mbps
<b><math>V_{CC}</math> Jitter Sensitivity</b>					
27 MHz		0.85	—	—	ns/V
270 MHz		1.90	—	—	ns/V
<b><math>V_{EE}</math> Jitter Sensitivity</b>					
27 MHz		0.55	—	—	ns/V
270 MHz		1.45	—	—	ns/V
<b>STATIC PERFORMANCE</b>					
<b>Supply Current (Includes Output Current)</b>					
$V_{AEC} = 0V$	(Note 3)	58	48/68	40/75	mA
$V_{AEC} = 0.4V$	(Note 3)	53	43/64	37/70	mA
<b>Input and Output Parameters</b>					
DO/ $\overline{DO}$ output current		10	8.7/11.3	8.0/12	mA
DO/ $\overline{DO}$ output voltage swing	$R_{collector} = 75\Omega$ (Note 3)	750	650/850	600/900	mV
DI/ $\overline{DI}$ common mode voltage		3.4	—	—	V
AEC differential voltage	Belden 8281	1.5	—	—	mV/meter
AEC+/AEC- common mode		3.6	—	—	V
output eye monitor (OEM) bias potential		3.2	—	—	V
carrier detect (CD) current output-HIGH	CD $V_{OH} = 4.5V$	-400	—	—	$\mu$ A
carrier detect (CD) current output-LOW	CD $V_{OL} = 0.5V$	600	—	—	$\mu$ A
MUTE voltage input-HIGH	(Note 3)	1.8	2.0	2.0	V
MUTE voltage input-LOW	(Note 3)	1.2	0.8	0.8	V

## Electrical Characteristics (Continued)

( $V_{CC} = +5V$ ,  $V_{EE} = 0V$ , signal source swing =  $0.8 V_{pp}$ (Note 4),  $C_{AEC} = 100 \text{ pF}$ )

Parameter	Conditions	Typ +25°C	Min/Max +25°C	Min/Max -40°C to +85°C	Units
<b>Input and Output Parameters</b>					
MUTE current input-HIGH	$V_{IH} = 5V$ (Note 3)	5.0	±100	±500	nA
MUTE current input-LOW	$V_{IL} = 0V$ (Note 3)	0.2	±100	±500	nA
<b>TIMING PERFORMANCE</b>					
<b>CD Response Time</b>					
carrier applied	(Note 8)	1.0	–	–	µs
carrier removed	(Note 9)	12	–	–	µs
MUTE response time	(Note 10)	2.0	–	–	ns
<b>MISCELLANEOUS PERFORMANCE</b>					
input resistance	single-ended	7.3	–	–	kΩ
input capacitance	single-ended (Note 11)	1.0	–	–	pF
input return loss @ 270 MHz	$Z_o = 75\Omega$ (Note 12)	19	–	–	dB
maximum cable attenuation	200 MHz (Note 13)	40	–	–	dB

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

**Note 3:** J-level: spec. is 100% tested at +25°C.

**Note 4:** These specifications assume an  $800 \text{ mV}_{pp}$  signal at the cable input. Levels above and below  $800 \text{ mV}$  are allowable, but performance may vary. The cable will attenuate the signal prior to entering the equalizer.

**Note 5:** Peak-to-peak jitter is defined as 6 times the rms jitter.

**Note 6:** For more information, see "CLC014 Operation" and "Design Guidelines".

**Note 7:** 50% eye opening.

**Note 8:** Time from application of a valid signal to when the CD output asserts high.

**Note 9:** Time from the removal of a valid signal to when the CD output asserts low.

**Note 10:** Time from assertion of MUTE to when the output responds.

**Note 11:** Device only. Does not include typical pc board parasitics.

**Note 12:** Includes typical pc board parasitics.

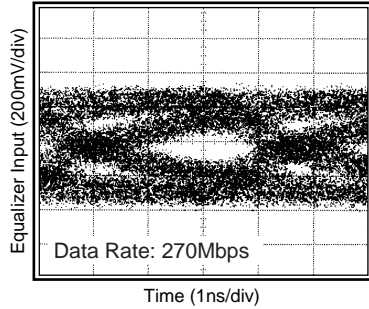
**Note 13:** This sets the maximum cable length for the equalizer.

**Note 14:** Human body model,  $1.5 \text{ k}\Omega$  in series with  $100 \text{ pF}$ ; based on limited test data.

**Note 15:** To maintain specified performance, do not reduce  $\overline{DO}/\overline{DO}$  below this level.

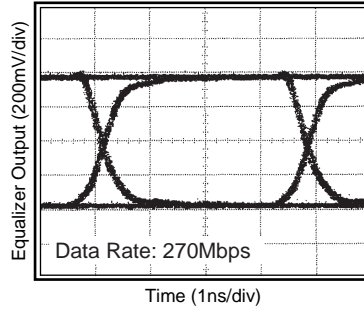
## Typical Performance Characteristics

**Before Equalization:**  
100m of Belden 8281 Coaxial Cable



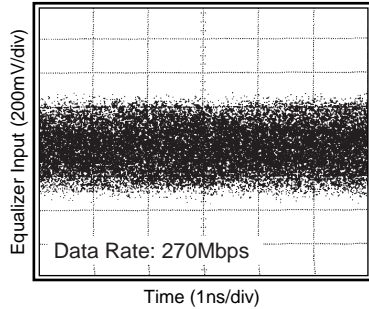
DS100056-5

**After Equalization:**  
100m of Belden 8281 Coaxial Cable



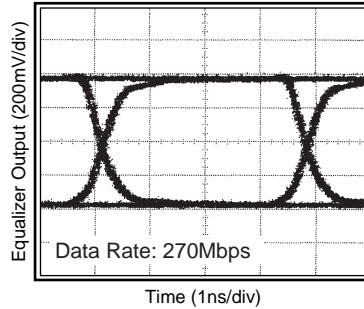
DS100056-8

**Before Equalization:**  
200m of Belden 8281 Coaxial Cable



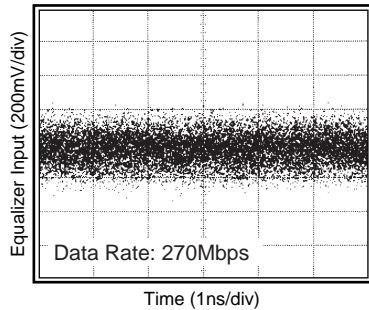
DS100056-6

**After Equalization:**  
200m of Belden 8281 Coaxial Cable



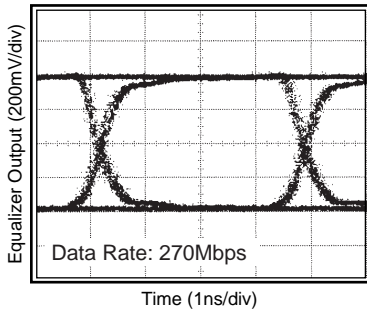
DS100056-9

**Before Equalization:**  
300m of Belden 8281 Coaxial Cable



DS100056-7

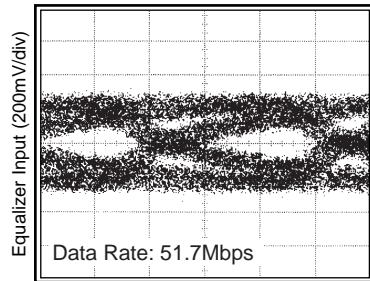
**After Equalization:**  
300m of Belden 8281 Coaxial Cable



DS100056-10

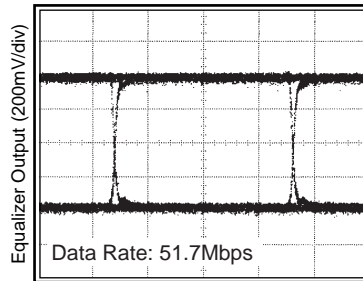
## Typical Performance Characteristics (Continued)

**Before Equalization:**  
100m Category 5 UTP at 51.7Mbps



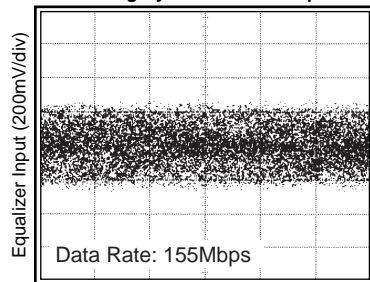
DS100056-11

**After Equalization:**  
100m Category 5 UTP at 51.7Mbps



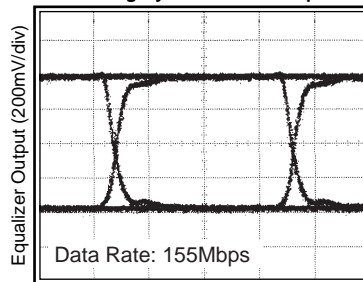
DS100056-14

**Before Equalization:**  
100m Category 5 UTP at 155Mbps



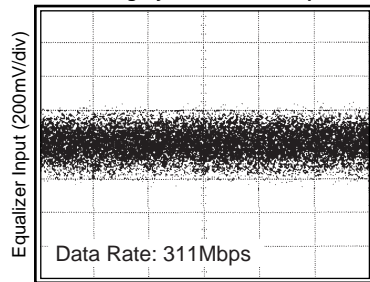
DS100056-12

**After Equalization:**  
100m Category 5 UTP at 155Mbps



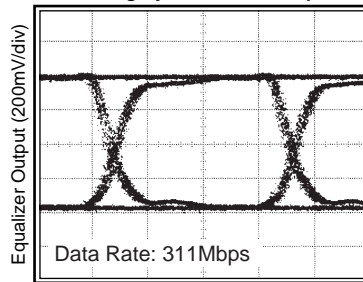
DS100056-15

**Before Equalization:**  
100m Category 5 UTP at 311Mbps



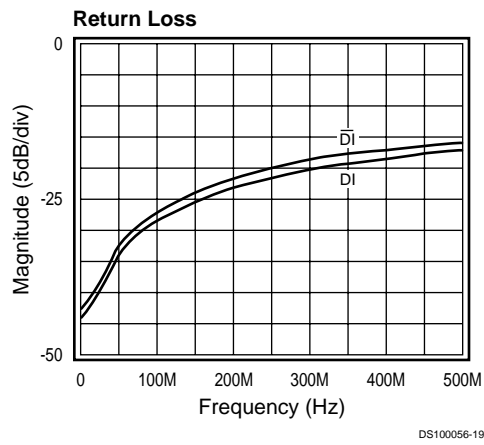
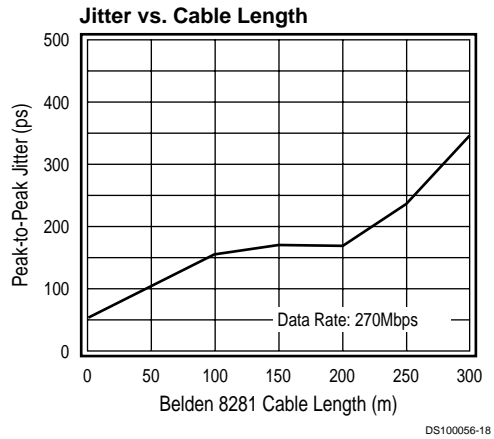
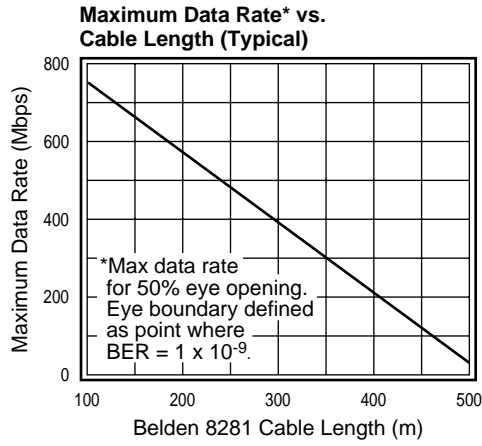
DS100056-13

**After Equalization:**  
100m Category 5 UTP at 311Mbps



DS100056-16

## Typical Performance Characteristics (Continued)



## Pin Definitions

Name	Pin #	Description
DI, $\overline{DI}$	8, 9	Differential data inputs.
DO, $\overline{DO}$	13, 14	Differential collector data outputs (ECL compatible).
AEC+, AEC-	6, 7	AEC loop filter pins. A capacitor connected between these pins governs the loop response for the adaptive equalization loop.
OEM	3	Eye monitor output. The output of the equalization filter.
CD	5	Carrier detect. (Low when no signal is present).
$\overline{MUTE}$	12	Output $\overline{MUTE}$ . (Active low.) Carrier detect may be tied to this pin to inhibit the output when no signal is present.
$V_{CC}$	1, 2, 4	Positive supply pins (ground or +5V).
$V_{EE}$	10, 11	Negative supply pins (-5.2V or ground).

## Operation

The CLC014 Adaptive Cable Equalizer provides a complete solution for equalizing high-bit-rate digital data transmitted over long transmission lines. The following sections furnish design and application information to assist in completing a successful design:

- Block diagram explanation of the CLC014
- Recommended standard input and output interface connections
- Common applications for the CLC014
- Measurement, PC layout, and cable emulation boxes

For applications assistance in the U.S., call 800-272-9959 to contact a technical staff member.

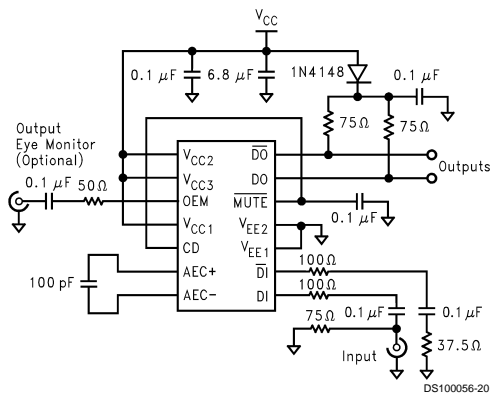


FIGURE 1. CLC014 Equalizer Application Circuit

## BLOCK DESCRIPTION

The CLC014 is an adaptive equalizer that reconstructs serial digital data received from transmission lines such as coaxial cable or twisted pair. Its transfer function approximates the reciprocal of the cable loss characteristic. The block diagram in *Figure 2* depicts the main signal conditioning blocks for equalizing digital data at the receiving end of a cable. The CLC014 receives baseband differential or single-ended digital signals at its inputs DI and  $\overline{DI}$ .

The **Equalizer** block is a two-stage adaptive filter. This filter is capable of equalizing cable lengths from zero meters to lengths that require 40 dB of boost at 200 MHz.

The **Quantized Feedback Comparator** block receives the differential signals from the equalizer filter block. This block includes two comparators. The first comparator incorporates a self-biasing DC restore circuit. This is followed by a second high-speed comparator with output mute capability. The second comparator receives and slices the DC-restored data. Its outputs DO and  $\overline{DO}$  are taken from the collectors of the output transistors. MUTE latches DO and  $\overline{DO}$  when a TTL logic low level is applied.

The **Adaptive Servo Control** block produces the signal for controlling the filter block, and outputs a voltage proportional to cable length. It receives differential signals from the output of the filter block and from the quantized-feedback comparator (QFBC) to develop the control signal. The servo loop response is controlled by an external capacitor placed across the AEC+ and AEC- pins. Its output voltage, as measured differentially across AEC+ and AEC-, is roughly proportional to the length of the transmission line. For Belden 8281 coaxial cable this differential voltage is about 1.5 mV/meter. Once this voltage exceeds 500 mV, no additional equalization is provided.

The **Carrier Detect (CD)** block monitors the signal power out of the equalizing filter and compares it to an internal reference to determine if a valid signal is present. A CMOS high output indicates that data is present. The output of CD can be connected to the  $\overline{MUTE}$  input to automatically latch the outputs (DO and  $\overline{DO}$ ), preventing random transitions when no data is present.

The **Output Eye Monitor (OEM)** provides a single-ended buffered output for observing the equalized eye pattern. The OEM output is a low impedance high-speed voltage driver capable of driving an AC-coupled 100 Ω load.

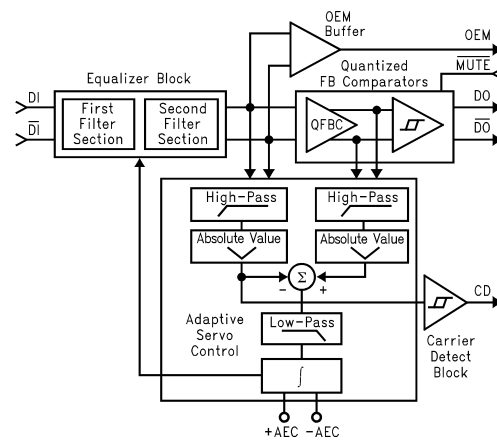


FIGURE 2. CLC014 Block Diagram



## Input Interfacing

The CLC014 accepts either differential or single-ended input voltage specified in **Static Performance**. The following sections show several suggestions for interfaces for the inputs and outputs of the CLC014.

### SINGLE-ENDED INPUT INTERFACE: 75Ω Coaxial Cable

The input is connected single-ended to either DI or  $\overline{\text{DI}}$  as shown in *Figure 3*. Balancing unused inputs helps to lessen the effects of noise. Use the equivalent termination of 37.5Ω to balance the input impedance seen by each pin. It also helps to terminate grounds at a common point. Resistors  $R_x$  and  $R_y$  are recommended for optimum performance. The equalizer inputs are self-biasing. Signals should be AC coupled to the inputs as shown in *Figure 3*.

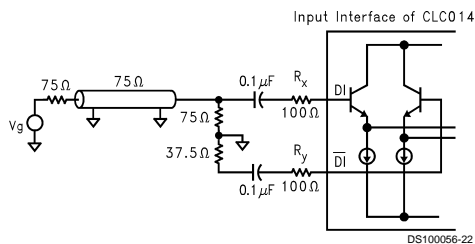


FIGURE 3. Single-Ended 75Ω Cable Input Interface

### DIFFERENTIAL INPUT INTERFACE: Twisted Pair

A recommended differential input interface is shown in *Figure 4*. Proper voltage levels must be furnished to the input pins and the proper cable terminating impedance must be provided. For Category 5 UTP this is approximately 100Ω. *Figure 4* shows a generalized network which may be used to receive data over a twisted pair. Resistors  $R_1$  and  $R_2$  provide the proper terminating impedance and signal level adjustment. The blocking capacitors provide AC coupling of the attenuated signal levels. The plots in the **Typical Performance Characteristics** section demonstrate various equalized data rates using Category 5 UTP at 100 meter lengths. A full schematic of a recommended driver and receiver circuit for 100Ω Category 5 UTP is provided in the **Typical Applications** section with further explanation.

$$R_1 = \frac{Z_o}{V_{pp}} \left( \frac{V_{pp} - 1.6}{2} \right) \quad R_2 = \frac{0.8Z_o}{V_{pp}}$$

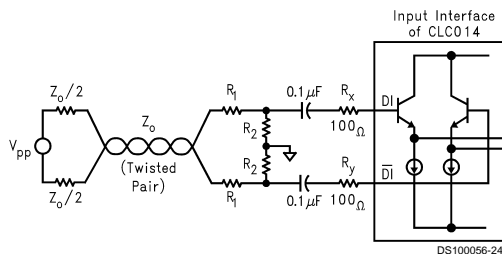


FIGURE 4. Twisted Pair Input Interface

## Output Interfacing

The outputs DO and  $\overline{\text{DO}}$  produce ECL logic levels when the recommended output termination networks are used. The

DO and  $\overline{\text{DO}}$  pins are **not complementary emitter coupled logic** outputs. Instead, the outputs are taken off of the collectors of the transistors. Therefore, care must be taken to meet the interface threshold levels required by ECL families. Recommended interfaces for standard ECL families are shown in the following circuits.

### DIFFERENTIAL LOAD-TERMINATED OUTPUT INTERFACE

*Figure 5* shows a recommended circuit for implementing a differential output that is terminated at the load. A diode and 75Ω resistor provides a voltage drop from the positive supply (+5V for PECL or Ground for ECL operation) to establish proper ECL levels. The resistors terminate the cable to the characteristic impedance. The output voltage swing is determined by the CLC014 output current (10 mA) times the termination resistor. For the circuit in *Figure 5*, the nominal output voltage swing is 750 mV.

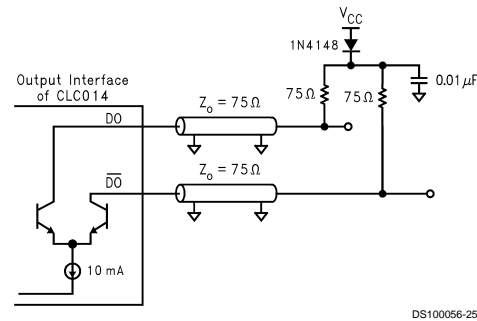


FIGURE 5. Differential Load Terminated Output Interface

### DIFFERENTIAL SOURCE-TERMINATED OUTPUT INTERFACE

*Figure 6* is similar to *Figure 5* except that the termination is provided at the source. This configuration may also be used for single-ended applications. However, the unused output must still be terminated as shown.

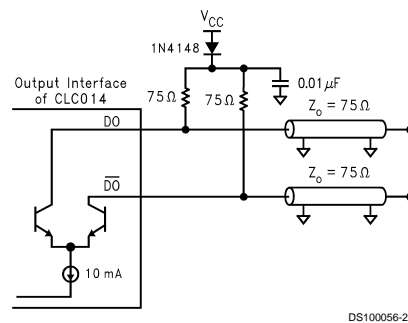


FIGURE 6. Differential Source Terminated Output Interface

### TERMINATING PHYSICALLY SEPARATED OUTPUTS

When the two outputs must be routed to physically separate locations, the circuit in *Figure 6* may be applied. Alternatively, if load termination is desired, the circuit in *Figure 7*

## Output Interfacing (Continued)

may be used. The resistive divider network provides 75Ω termination and establishes proper ECL levels. This circuit consumes slightly more power than the previous circuits.

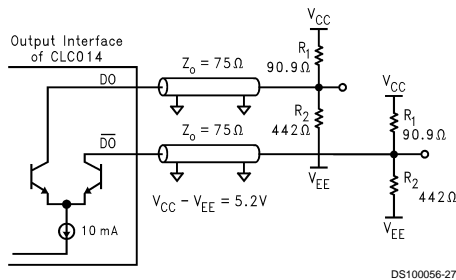


FIGURE 7. Alternative Load Terminated Output Interface

## Design Guidelines

### SELECTING THE AUTOMATIC EQUALIZER CAPACITOR

The AEC capacitor sets the loop time constant  $\tau$  for the equalizer's adaptive loop response time. The following formula is used to set the loop time constant:

$$\tau = R \cdot C_{AEC} \cdot 10^{-6}$$

R is a conversion factor that is set by internal equalizer parameters and cable length. For Belden 8281 coaxial cable, the R values are ( $\tau = \mu\text{s}$ ,  $C_{AEC}$  in pF):

Cable Length	R Value (Ohms)
100 meters	15000
200 meters	20000
300 meters	32000

For example, a  $C_{AEC}$  value of 100 pF results in an adaptive loop time constant of 2  $\mu\text{s}$  at 200 meters of cable.

### CONNECTION AND OPERATION OF CD AND MUTE

**Carrier Detect (CD)** is a CMOS output that indicates the presence of equalized data from the filter. This CD output can be connected to  $\overline{\text{MUTE}}$  to suspend changes in the data outputs DO and  $\overline{\text{DO}}$ , if no valid signal exists. This simple configuration prevents random output transitions due to noise. For sparse transition patterns it is recommended that a capacitor be connected to CD as shown in *Figure 1*.

Add a capacitor to pin 5 to slow the response time of Carrier Detect when Carrier Detect is connected to  $\overline{\text{MUTE}}$ . The capacitor reduces sensitivity to pathological patterns. Pathological patterns are defined as sparse data sequences with few transitions.

### OUTPUT EYE MONITOR OEM CONNECTIONS

The OEM is a high-speed, buffered output for monitoring the equalized eye pattern prior to the output comparator. Its output is designed to drive an AC-coupled 50Ω coaxial cable with a series 50Ω backmatch resistor. The cable should be terminated with 50Ω at the oscilloscope. *Figure 1* shows a schematic with a typical connection.

### MINIMUM DATA TRANSITIONS

The CLC014 specifies a minimum transition rate. For the CLC014 this sets the minimum data rate for transmitting data through any cable medium. The CLC014 minimum average transition density is found in the Electrical Characteristics section of the datasheet.

### POWER SUPPLY OPERATION AND THERMAL CONSIDERATIONS

The CLC014 operates from either +5V or -5.2V single supplies. Refer to *Figure 1* when operating the part from +5V. When operating with a -5.2V supply, the  $V_{EE}$  pins should be bypassed to ground. The evaluation board and associated literature provide for operation from either supply.

Maximum power dissipation occurs at minimum cable length. Under that condition,  $I_{CC} = 58 \text{ mA}$ .

Total power dissipated:

$$P_T = (58 \text{ mA})(5V) = 290 \text{ mW}$$

Power in the load:

$$P_L = (0.7V)(11 \text{ mA}) + (37.5)(11 \text{ mA})^2 = 12 \text{ mW}$$

Maximum power dissipated on the die:

$$P_{D\text{MAX}} = P_T - P_L = 278 \text{ mW}$$

Junction Temperature =

$$(\theta_{JA})(278 \text{ mW}) + T_A = T_A + 26^\circ\text{C}$$

## Layout and Measurement

The printed circuit board layout for the CLC014 requires proper high-speed layout to achieve the performance specifications found in the datasheet. The following list contains a few rules to follow:

1. Use a ground plane.
2. Decouple power pins with 0.1  $\mu\text{F}$  capacitors placed  $\leq 0.1''$  (3mm) from the power pins.
3. Design transmission strip lines from the CLC014's input and output pins to the board connectors.
4. Route outputs away from inputs.
5. Keep ground plane  $\geq 0.025''$  (0.06mm) away from the input and output pads.

Figure 8 shows a block level measurement diagram, while Figure 15 on depicts a detailed schematic. A pseudo-random pattern generator with low output jitter was used to provide a NRZI pattern to create the eye diagrams shown in the **Typical Performance Characteristics** section.

Since most pattern generators have a 50 $\Omega$  output impedance, a translation can be accomplished using a CLC006 Cable Driver as an impedance transformer. A wide bandwidth oscilloscope is needed to observe the high data rate eye pattern. When monitoring a single output that is terminated at both the equalizer output and the oscilloscope, the effective output load is 37.5 $\Omega$ . Consequently, the signal swing is half that observed for a single-ended 75 $\Omega$  termination.

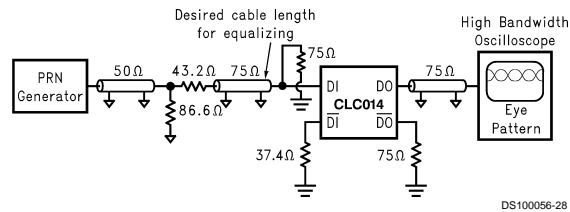


FIGURE 8. Typical Measurement Block

Troubleshooting with scope probes can affect the equalization. For high data rates, use a **low capacitance probe** with less than 2 pF probe capacitance. Evaluation boards and literature are available for quick prototyping and evaluation of the CLC014 Adaptive Cable Equalizer. The CLC014 contains CMOS devices and operators should **use grounding straps when handling** the parts.

Figure 9 shows the CLC014's internal power supply routing. Bypass  $V_{CC}$  (pin 4) by:

- Monolithic capacitor of about 0.1  $\mu\text{F}$  placed less than 0.1" (3mm) from the pin
- Tantalum capacitor of about 6.8  $\mu\text{F}$  for large current signal swings placed as close as convenient to the CLC014

Several layout techniques can improve high speed performance:

- Keep input, output and AEC traces well separated
- Use balanced input termination's
- Avoid routing traces close to the CLC014's input trace
- Maintain common return points for components
- Use guard traces

The input lines of the CLC014 use a 100 $\Omega$  series resistors at the input pins. This decreases the inductive effects internal to the part to reduce ringing on fast rise and fall times. Refer to the evaluation board layout for further suggestions on layout for the CLC014 Adaptive Equalizer.

### EQUALIZATION CURVE

The CLC014 Adaptive Cable Equalizer has a maximum equalization response as shown in Figure 10. This response may be obtained by forcing  $>0.5\text{V}$  differentially at the AEC pins.

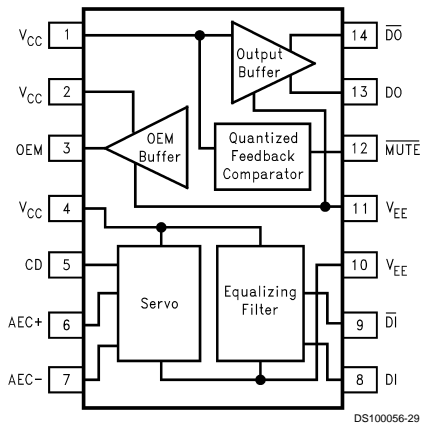
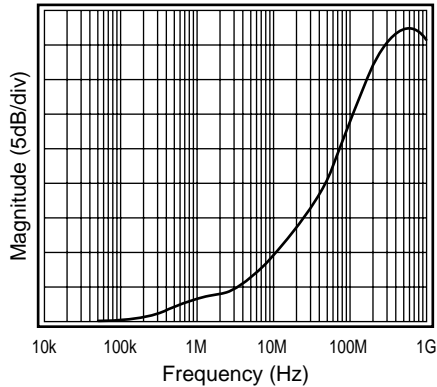


FIGURE 9. Power Package Routing Fixture

To minimize ringing at the CLC014's inputs, place a 100 $\Omega$  resistor in series with the input. This resistor reduces inductance effects.

## Layout and Measurement (Continued)



DS100056-30

FIGURE 10. Maximum Equalization Response

### CABLE EMULATION BOXES

Some cable emulation boxes will not mimic cables correctly. When evaluating the CLC014, it is strongly recommended that actual cable be used to determine the various performance parameters.

## Typical Applications

### COAXIAL CABLE RECEIVER (Page 1)

The CLC014 equalizer application shown on page 1 will equalize a variety of coaxial cables up to lengths that attenuate the signal by 40 dB at 200 MHz. The application shows the proper connection for a single cable driven with a CLC006 driver. Carrier Detect (CD) is connected to MUTE to latch outputs DO and  $\overline{DO}$  in the absence of an input signal to the equalizer.

Refer to the CLC014's evaluation board layout for additional suggestions.

National can supply most of the major components required to design a transmission line repeater. Figure 11 shows a typical repeater design using the CLC006, CLC014, and the CLC016. The design functions supported by each chip are:

#### CLC006: Cable connection chip

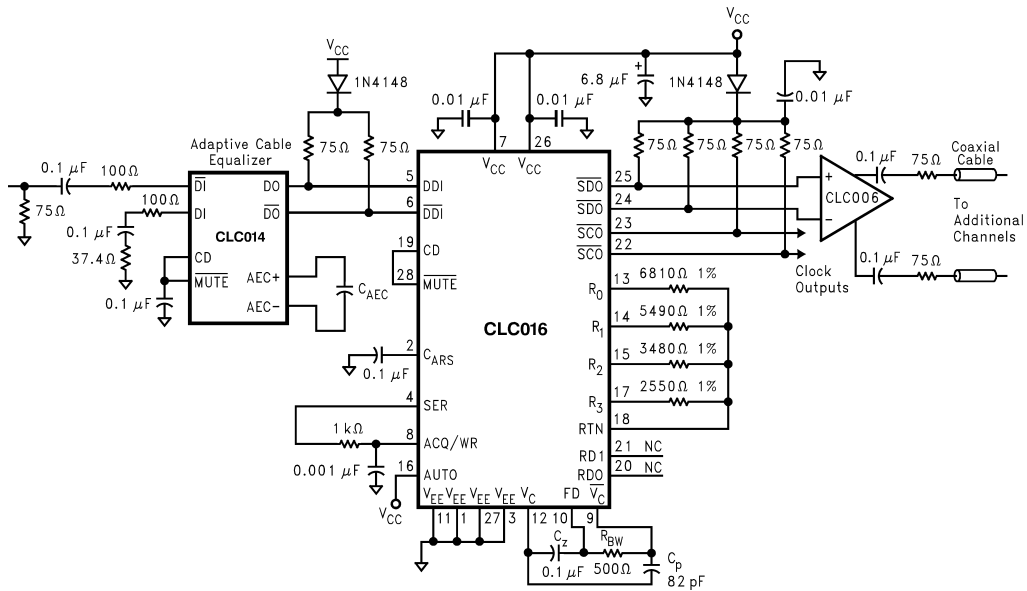
Boosts drive for transmission to next repeater or final destinations

#### CLC014: Receive serialized digital data from incoming transmission lines

Equalizes the incoming data

#### CLC016: Retimes the equalized data (improving jitter)

The CLC016 is a multi-rate data retiming PLL. The circuit (Figure 11) will work at up to 4 different data rates with no additional components or manual tuning.



DS100056-31

FIGURE 11. Typical Repeater Design

### DIGITAL VIDEO (SDV) ROUTERS

The CLC014 provides performance that complies with the SMPTE 259M standard for serial digital video (SDV) transmission over coaxial cable. One common application is in

SDV routers, which provide a switching matrix for connecting video source equipment (e.g., cameras) to destination equipment (e.g., video tape recorders, monitors, etc.).

Figure 12 shows a typical configuration for an SDV router, including equalizers, a crosspoint switch, data retimers, and cable drivers. The CLC014 is used in its standard configura-

## Typical Applications (Continued)

tion in this application, and automatically equalizes cable lengths from zero meters to greater than 300 meters at 360 MHz (see plots in **Typical Performance Characteristics** section). The equalized outputs are connected to the differential inputs of the crosspoint switch. The CLC016 Data Retimer receives the data from the crosspoint and performs the clock and data recovery functions, further reducing jitter. Finally, the retimed data is driven into the coaxial cable by a CLC006 Cable Driver (with two amplitude-adjustable outputs) or a CLC007 Cable Driver (with four outputs).

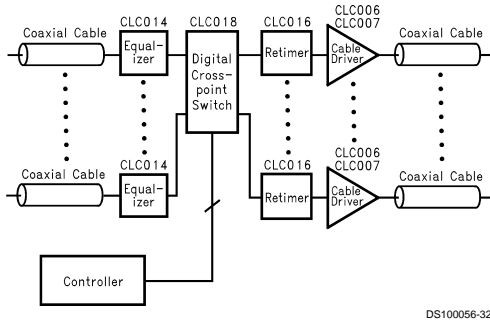


FIGURE 12. Video Routing Block Diagram

### TWISTED PAIR DRIVER

A low-cost medium for transmitting data is twisted pair. Category 5 UTP has an attenuation characteristic similar to Belden 8281 coaxial cable but scaled in length: 120 meters of Category 5 UTP is roughly equivalent to 300 meters of Belden 8281 cable. When properly implemented, the CLC014 will equalize data rates up to 625 Mbps over Category 5 UTP. The maximum data rate depends upon the cable length. A plot of Maximum Data Rate vs Cable Length is found in the **Typical Performance Characteristics** section for Belden 8281, and can be scaled as stated above to estimate maximum cable lengths and data rates for UTP.

Category 5 UTP has a characteristic impedance of approximately  $100\Omega$ . The CLC006 in Figure 13 is used to drive the twisted pair AC-coupled with a series  $0.1\mu\text{F}$  capacitor and a  $50\Omega$  resistor in each differential output. The CLC014 Adaptive Equalizer requires  $800\text{mV}_{\text{pp}}$  from the transmit side of

the cable. A voltage divider is necessary to scale the voltage to the required level at the input of the CLC014. This resistor network also provides the correct impedance match for twisted pair.

For Category 5 UTP, the approximate AEC voltage per length is  $3.75\text{mV/m}$  (see **Block Description**). The CLC006 provides a trim adjust for fine tuning the output signal with the resistor R. Refer to the CLC006/007 datasheet for tuning directions.

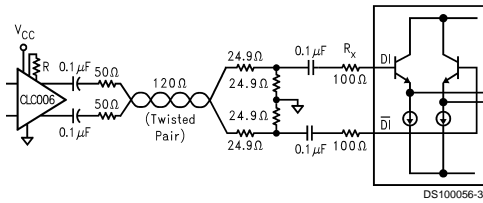


FIGURE 13. Twisted Pair Equalization

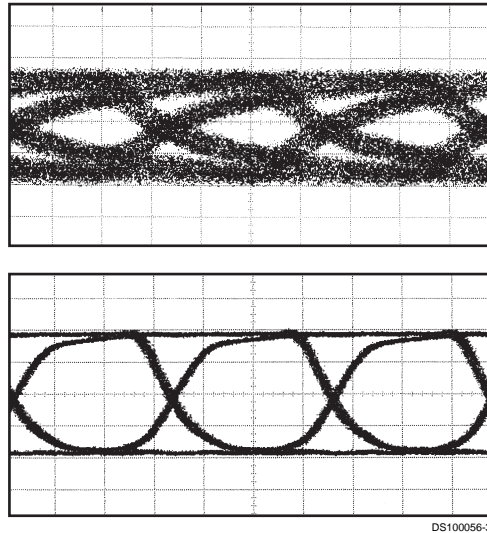


FIGURE 14. Before and After Equalization at 622 Mbps Through 50 Meters of Category 5 UTP

## Typical Applications (Continued)

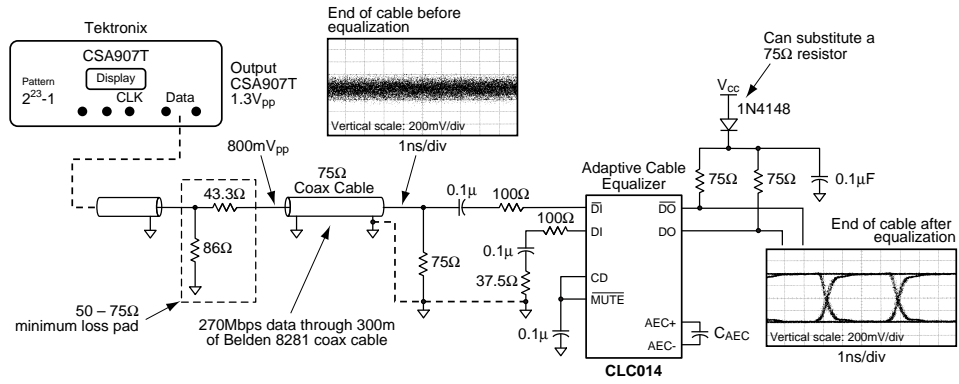


FIGURE 15. Typical Measurement Setup

## Evaluation Board

An evaluation board layout and schematic are shown on the following pages. The artwork shows the board solder masks, trace layers, and ground plane. To order an evaluation board contact your local sales representative or National support center and request part number CLC730063.

The evaluation board provides an LED and switches to operate the CLC014 in various modes of operation. The power

supplies, which must be correctly connected and jumpered for positive or negative voltage operation, are identified on the printed board silk screen. Insert all tantalum capacitors as shown in the schematic or silk screen. A complete bill of materials is given in the accompanying table. The components recommended in the materials list are SMPTE 259M standard.

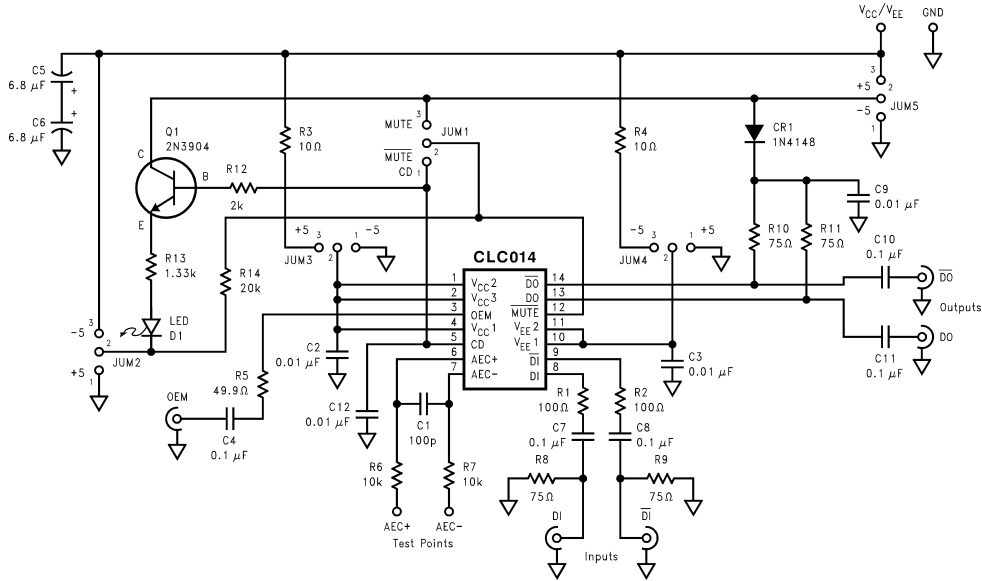


FIGURE 16. Evaluation Board Schematic

DS100056-36

## Evaluation Board (Continued)

### CLC014 Equalizer Evaluation Board

Item	Reference Designator	Description	Quantity
1	Q1	2N3904 transistor	1
2	CR1	1N4148 switching diode	1
3	J1, J2, J3, J4, J5	receptacle vertical BNC PC Amphenol #31-5329-52RFX	5
4	J6	banana jack, black, EF Johnson #108-0903-001	1
5	J7	banana jack, red, EF Johnson #108-0902-001	1
6	R6, R7	10 k $\Omega$ , 1/8W, 1206, 1% chip resistors	2
7	R8, R9, R10, R11	75 $\Omega$ , 1/8W, 1206, 1% chip resistors	4
8	R13	1.33 k $\Omega$ , 1/8W, 1206, 1% chip resistors	1
9	R3, R4	10 $\Omega$ , 1/8W, 1206, 1% chip resistors	2
10	R1, R2	100 $\Omega$ , 1/8W, 1206, 1% chip resistors	2
11	R14	20 k $\Omega$ , 1/8W, 1206, 1% chip resistors	1
12	R12	2 k $\Omega$ , 1/8W, 1206, 1% chip resistors	1
13	R5	49.9 $\Omega$ , 1/8W, 1206, 1% chip resistors	1
14	C2, C3, C9, C12	0.01 $\mu$ Fd, 10% X7R surface mount cap	3
15	C4, C7, C8, C10, C11	0.1 $\mu$ Fd, 10% X7R surface mount cap	5
16	C1	100 pFd, 5% NPO surface mount cap	1
17	C5, C6	6.8 $\mu$ Fd, 16V tantalum capacitor	2
18		CLC730063 printed circuit board	1
19	U1	CLC014AJE	1
20	D1	LED, GENERAL PURPOSE	1

#### LAYOUT

The CLC014 requires proper high-speed layout techniques to obtain best results. A few recommended layout rules to follow for best results when using the CLC014 Adaptive Cable Equalizer are:

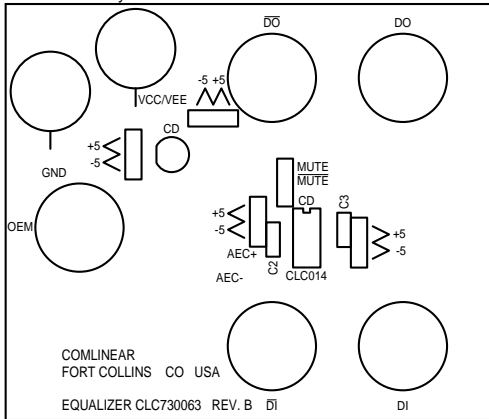
1. Use a ground plane.
2. Decouple power pins with 0.01  $\mu$ F capacitors placed  $\leq 0.1$ " (3mm) from the power pins.
3. Design transmission lines to the inputs and outputs.
4. Route outputs away from inputs.
5. Remove ground plane  $\geq 0.025$ " (0.06mm) from the input and output pads.

The solder masks with component locations, trace layer, and ground plane board layer are shown next.

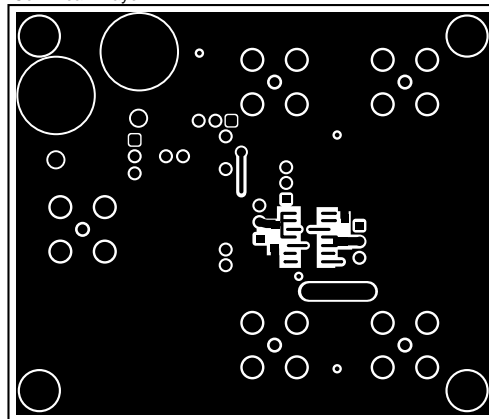


# Evaluation Board (Continued)

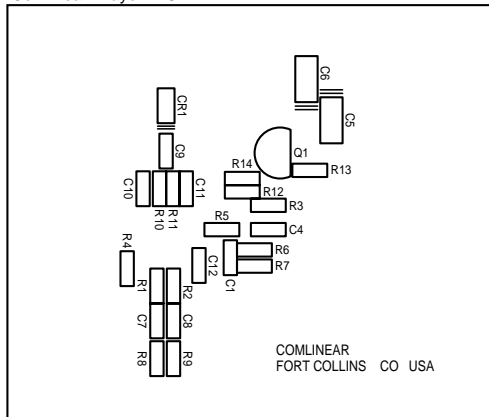
Comlinear Layer1 Silk



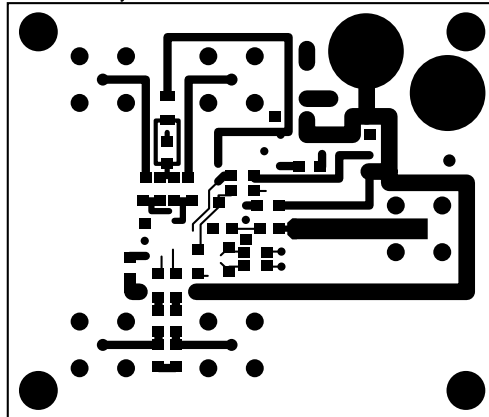
Comlinear Layer1



Comlinear Layer2 Silk

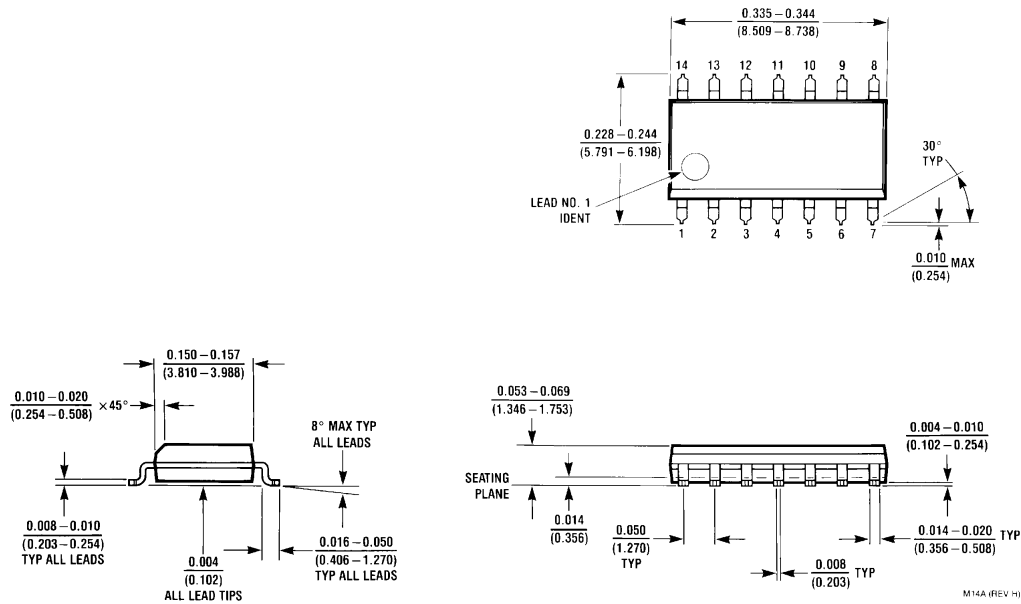


Comlinear Layer2



DS100056-37

**Physical Dimensions** inches (millimeters) unless otherwise noted




**14-Pin SOIC**  
**Order Number CLC014AJE**  
**NS Package Number M14A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 <p><b>National Semiconductor Corporation</b>  Americas  Tel: 1-800-272-9959  Fax: 1-800-737-7018  Email: support@nsc.com</p> <p>www.national.com</p>	<p><b>National Semiconductor Europe</b></p> <p>Fax: +49 (0) 1 80-530 85 86  Email: europe.support@nsc.com</p> <p>Deutsch Tel: +49 (0) 1 80-530 85 85  English Tel: +49 (0) 1 80-532 78 32  Français Tel: +49 (0) 1 80-532 93 58  Italiano Tel: +49 (0) 1 80-534 16 80</p>	<p><b>National Semiconductor Asia Pacific Customer Response Group</b></p> <p>Tel: 65-2544466  Fax: 65-2504466  Email: sea.support@nsc.com</p>	<p><b>National Semiconductor Japan Ltd.</b></p> <p>Tel: 81-3-5620-6175  Fax: 81-3-5620-6179</p>
--	---	---	---

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.